PE-APB

AMBA Advanced Peripheral Bus

OVERVIEW

The PE-APB is used to connect low speed peripheral in AMBA bus system. This IP also support to configure read-only memory space. The contents of memory are protected from changes.

FEATURES

The PE-APB includes the following features:

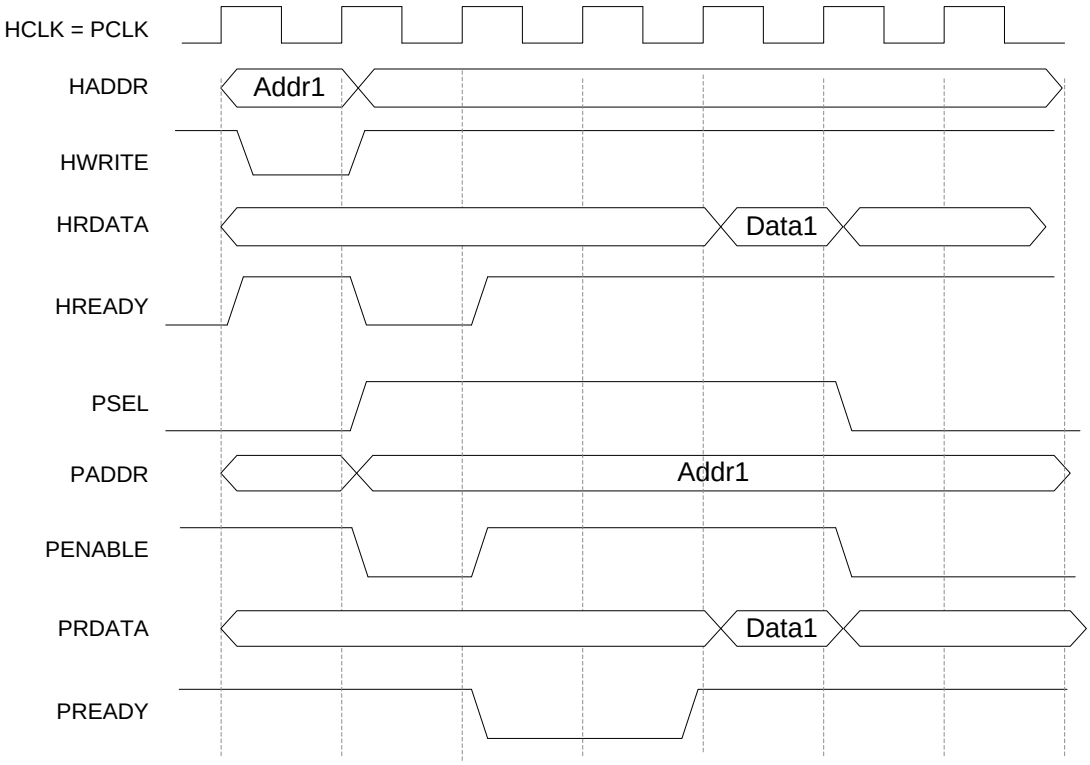
- Compliance with the AMBA Specification, Revision 2.0 from ARM.
- AHB slave

Support for the following:

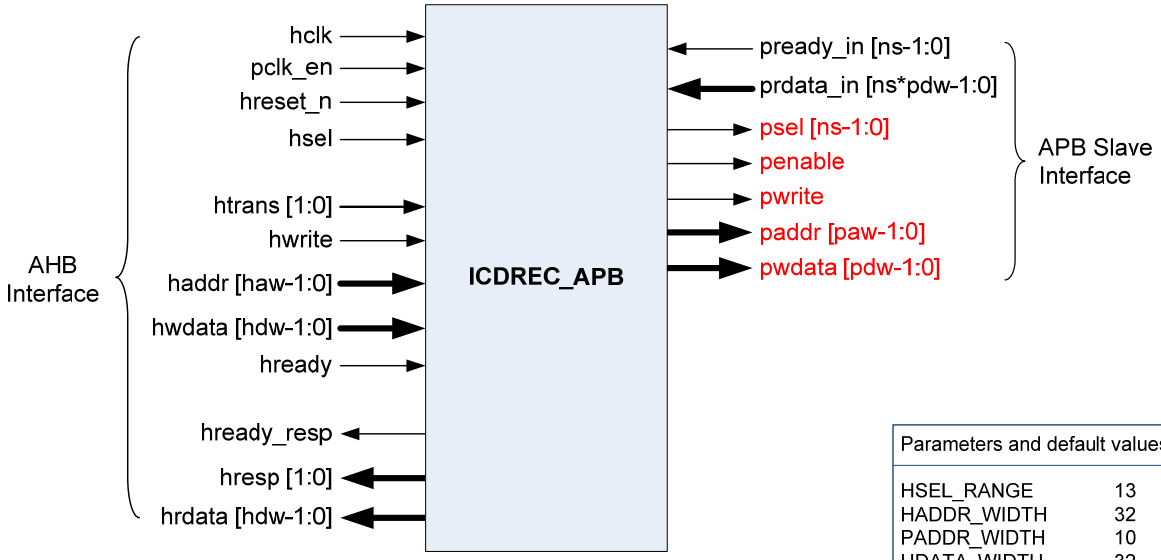
- Up to 16 APB slaves
- 32, 64, 128, and 256-bit AHB data buses
- 8, 16, and 32-bit APB data buses
- Single and burst AHB transfers
- Synchronous hclk/pclk; hclk is an integer multiple of pclk
- Big- and little-endian AHB systems
- Little-endian/Big-endian APB slave
- Read/Write on separate buses
- Configurable address bus width greater than 1KB and lower than APB bus address range, maximum 32 bit.
- Valid pready detection for APB slave

FUNCTIONAL DESCRIPTION

Read from APB bus to AHB bus timing



PORT DESCRIPTION



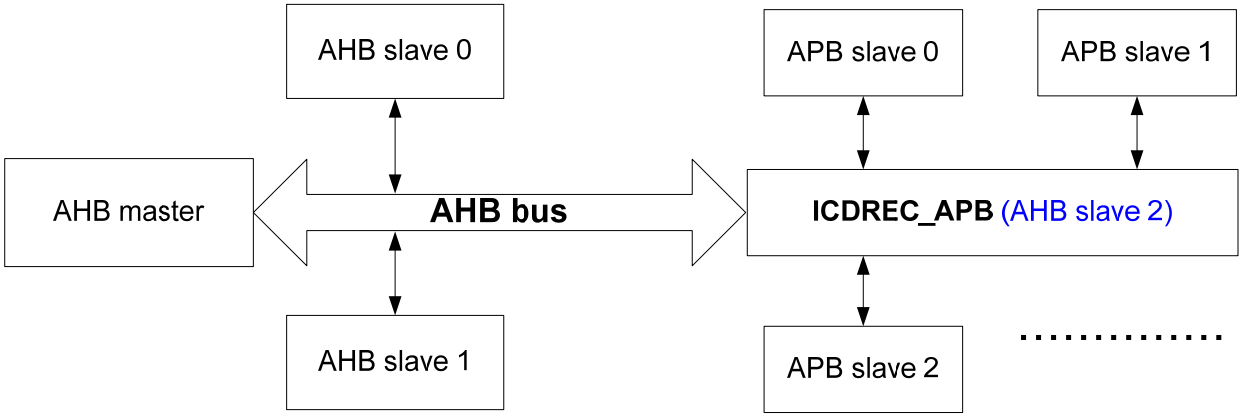
haw = width of AHB addres bus
hdw = width of the AHB data bus (max. value is 256 bits)
paw = width of the APB address bus
pdw = width of the APB data bus (max. value is 32 bits)
i = number associated with each APB slave (0 to 15)
ns = number of APB slave
Signals in red are registered.

Parameters and default values	
HSEL_RANGE	13
HADDR_WIDTH	32
PADDR_WIDTH	10
HDATA_WIDTH	32
PDATA_WIDTH	32
NUM_CHIP_SEL	4
AHB_BIG_ENDIAN	0
APB_BIG_ENDIAN	0
PROTECT_EN	0

I/O ports list

Group	Port	Width	Direction	Active	Description
Global	hclk	1	In	Positive trigger	System clock
	pclk_en	1	In	High	Peripheral bus clock enable
	reset_n	1	In	Low	Synchronous resets
AHB	hsel	1	In	High	AHB slave select
	htrans	2	In	-	Transfer type from selected master
	hwrite	1	In	-	When hwrite is high, this is write transfer. Reversely, this is read transfer.
	haddr	32	In	-	Address bus from AHB master
	hwdata	32	In	-	Write data bus from selected AHB master
	hready	1	In	High	Ready response from AHB bus
	hready_resp	1	Out	High	Ready response to AHB bus
	hresp	2	Out	-	Transfer Response
	hrdata	32	Out	-	Transfer data to AHB bus
APB	pready_in	ns	In	High	Ready respond from APB slaves
	prdata_in	ns*pdw	In	High	Read data from APB slaves
	psel	ns	Out	High	APB slave select
	penable	1	Out	High	APB slave enable
	pwrite	1	Out	-	When pwrite is high, this is write transfer. Reversely, this is read transfer.
	paddr	paw	Out	-	APB transfer address bus
	pwdata	pdw	Out	-	APB transfer write data bus

INTEGRATION



IMPLEMENTATION RESULTS

The design is synthesized with Number of APB slaves: 4.

Device	Logic	Memory bit	Fmax	DSP
Cyclone II: EP2C35F672C6	273	126	171.26MHz	
Cyclone III: EP3C40F780C6	273	126	198.97MHz	
Stratix II: EP2S60F672C3	151	126	270.05MHz	
Stratix III: EP3SL150F1152C2	153	126	447.43MHz	

DELIVERABLES

- Post-Synthesis netlist or source code
- Verilog testbench and test environment (if there are requests from customer)
- Technical document includes: user manual, datasheet, application note (optional)
- 1 Year warranty
- 60 days of technical support staring with the first incident, but limit to 6 months are included

ORDERING INFORMATION

For any modification or special request, please contact to ICDREC:

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